

FIG. 1

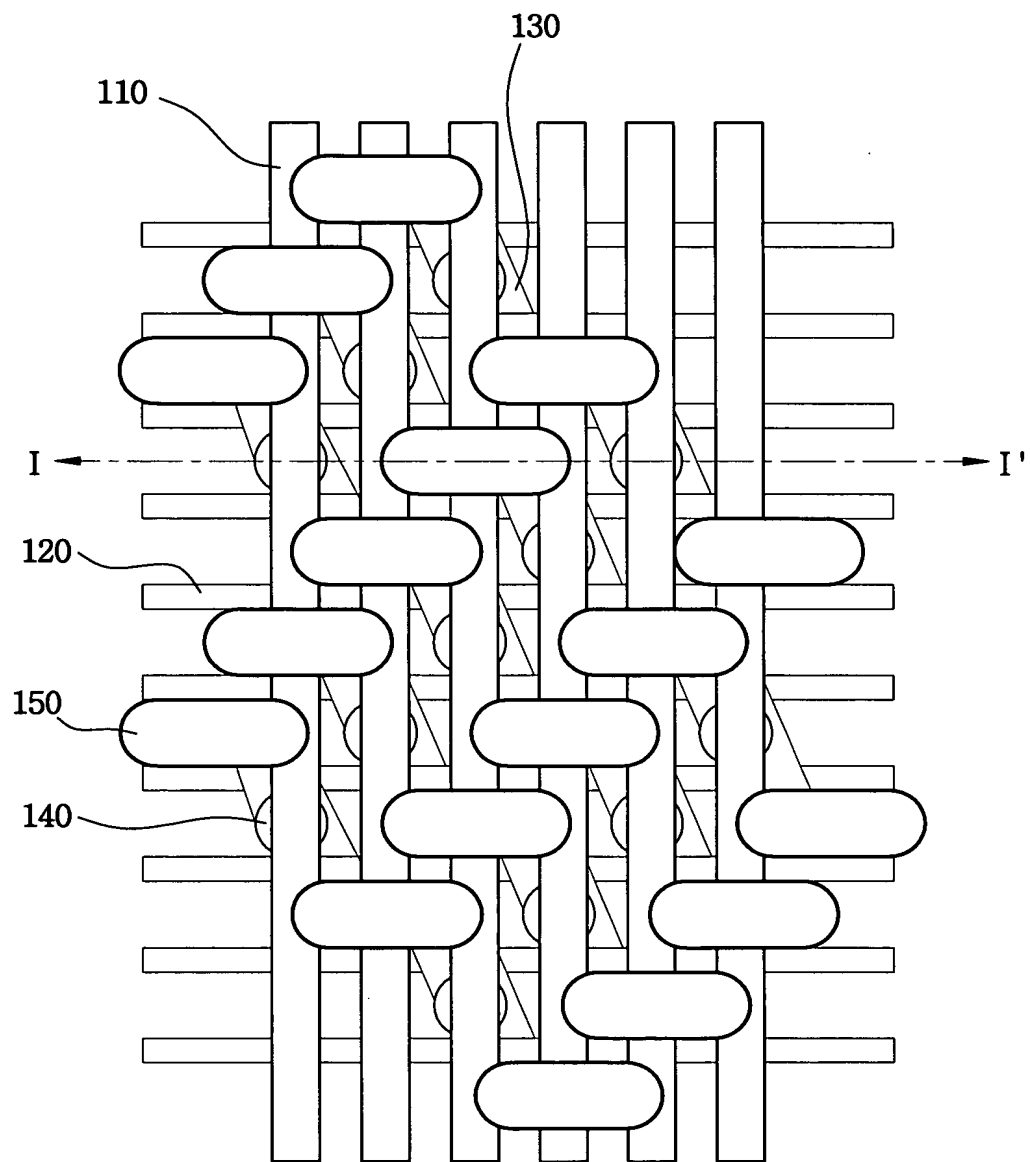


FIG. 2A

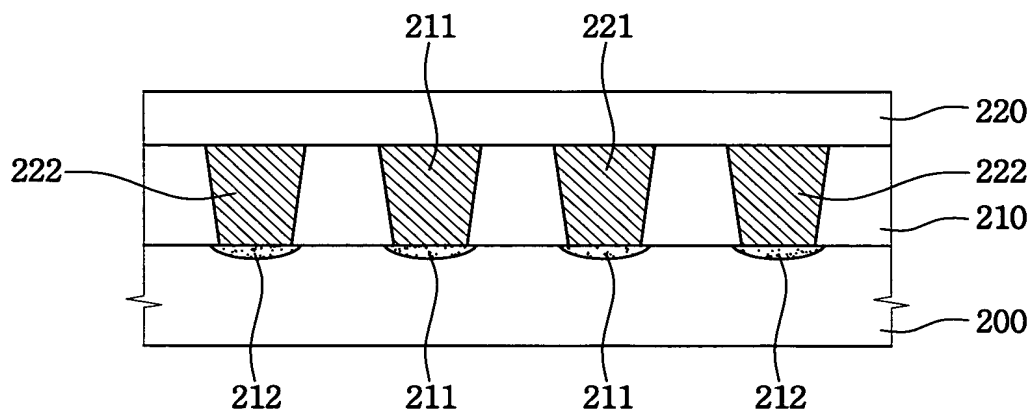
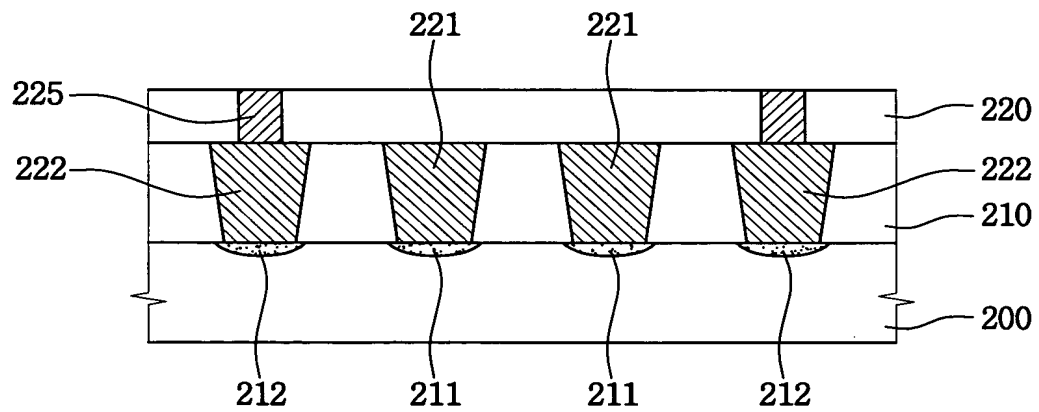


FIG. 2B



[illegible]

This cross-sectional view shows a central gate structure 260 on a substrate 200. The gate structure 260 includes a gate dielectric 246 and a gate electrode 245. The gate electrode 245 is surrounded by a gate sidewall 245. The gate structure 260 is positioned over a channel region 210. The channel region 210 is defined by a gate dielectric 211 and a gate electrode 212. The channel region 210 is surrounded by a gate sidewall 211. The gate structure 260 is positioned over a channel region 210. The channel region 210 is defined by a gate dielectric 211 and a gate electrode 212. The channel region 210 is surrounded by a gate sidewall 211. The gate structure 260 is positioned over a channel region 210. The channel region 210 is defined by a gate dielectric 211 and a gate electrode 212. The channel region 210 is surrounded by a gate sidewall 211.

FIG. 2E

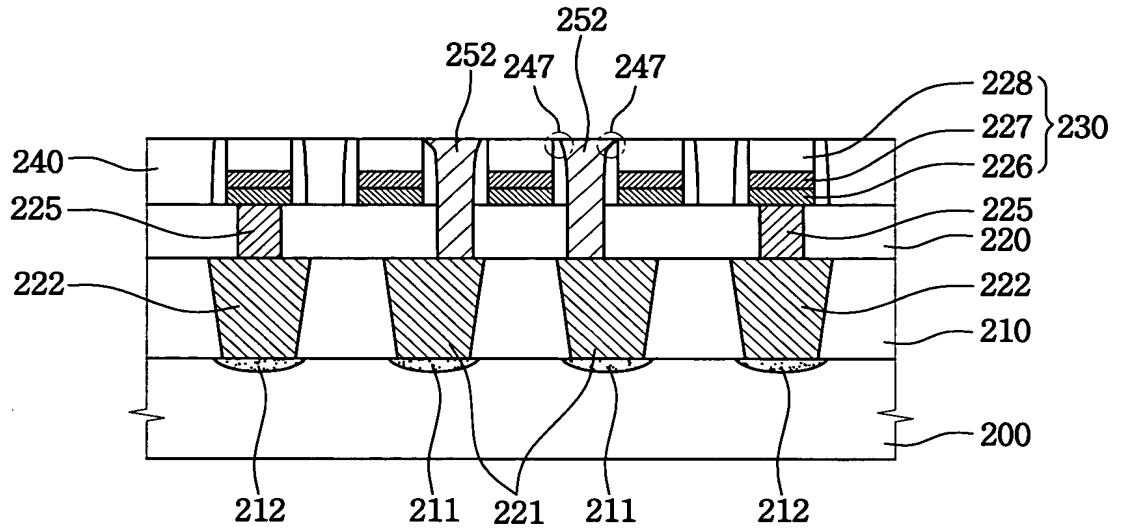


FIG. 2F

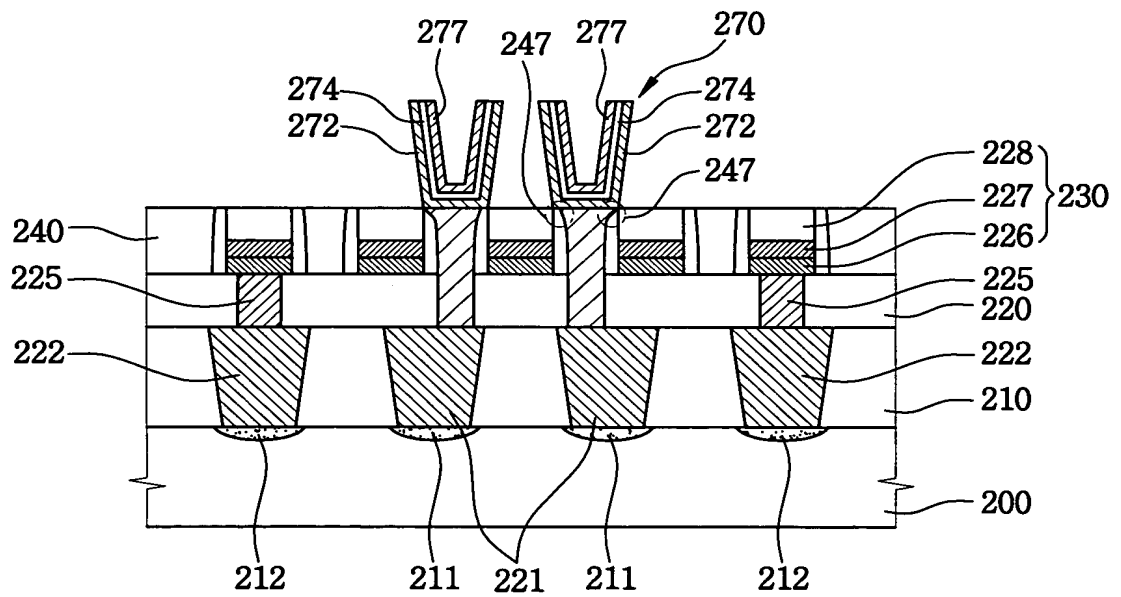


FIG. 3A

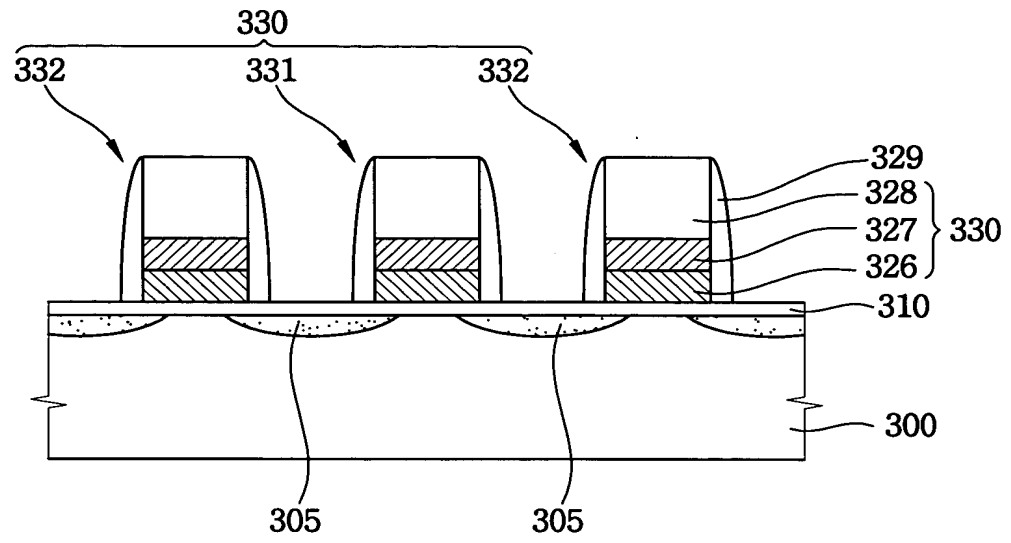


FIG. 3B

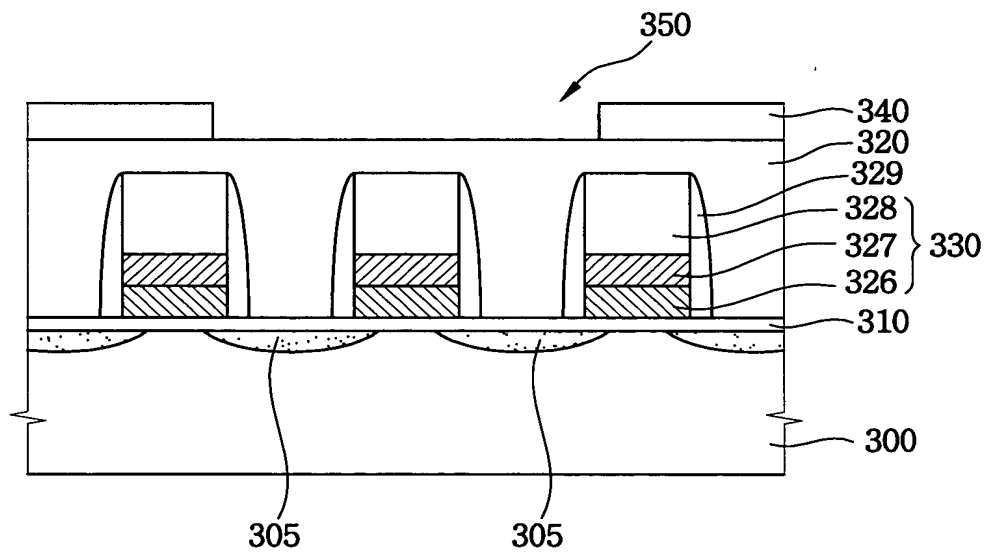


FIG. 3C

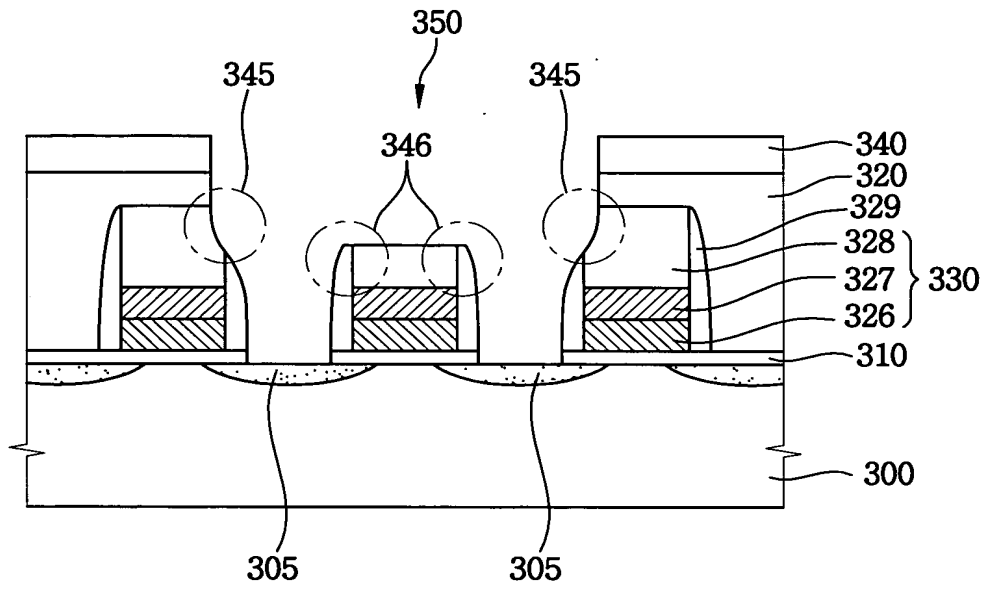


FIG. 3D

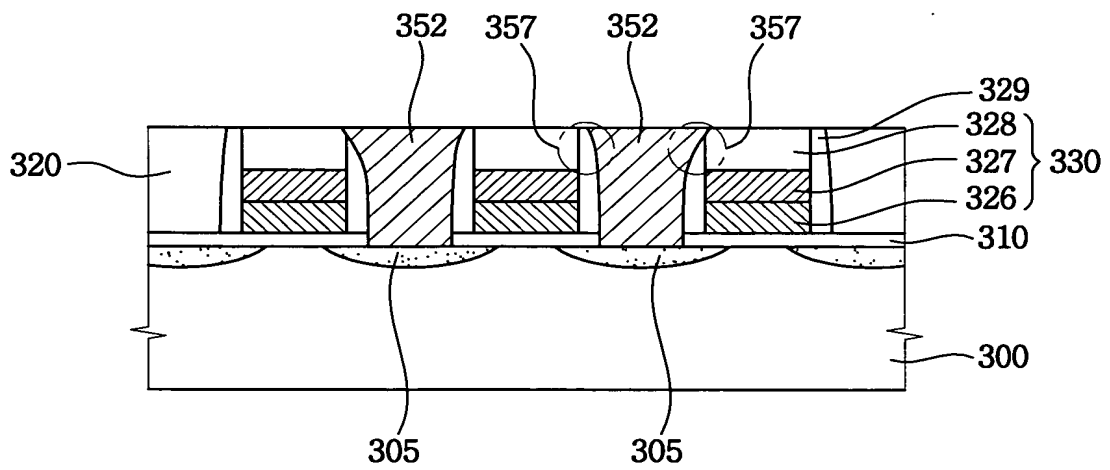


FIG. 3E

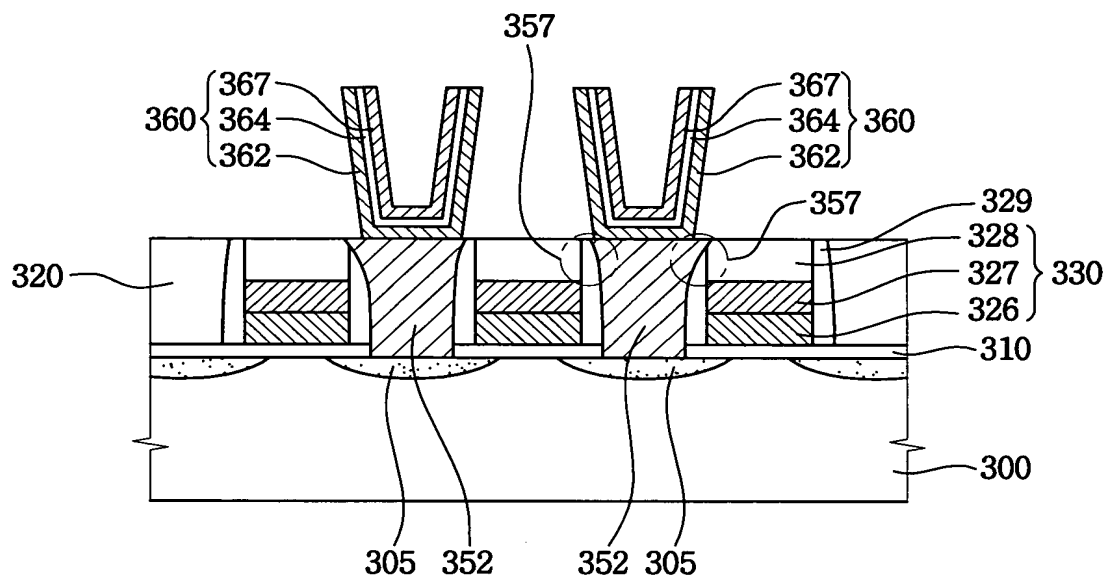


FIG. 4A

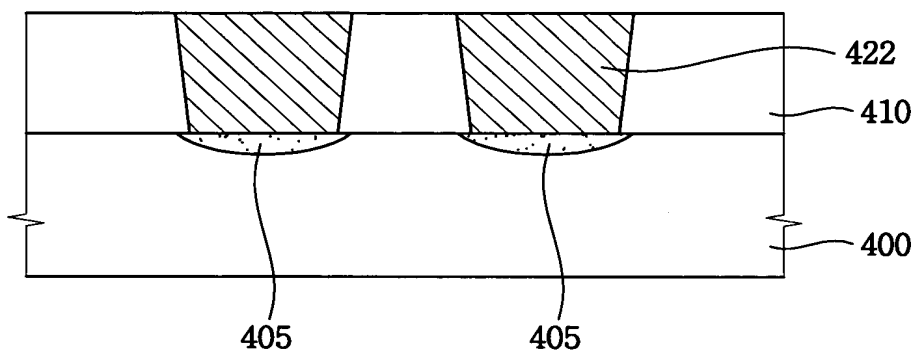


FIG. 4B

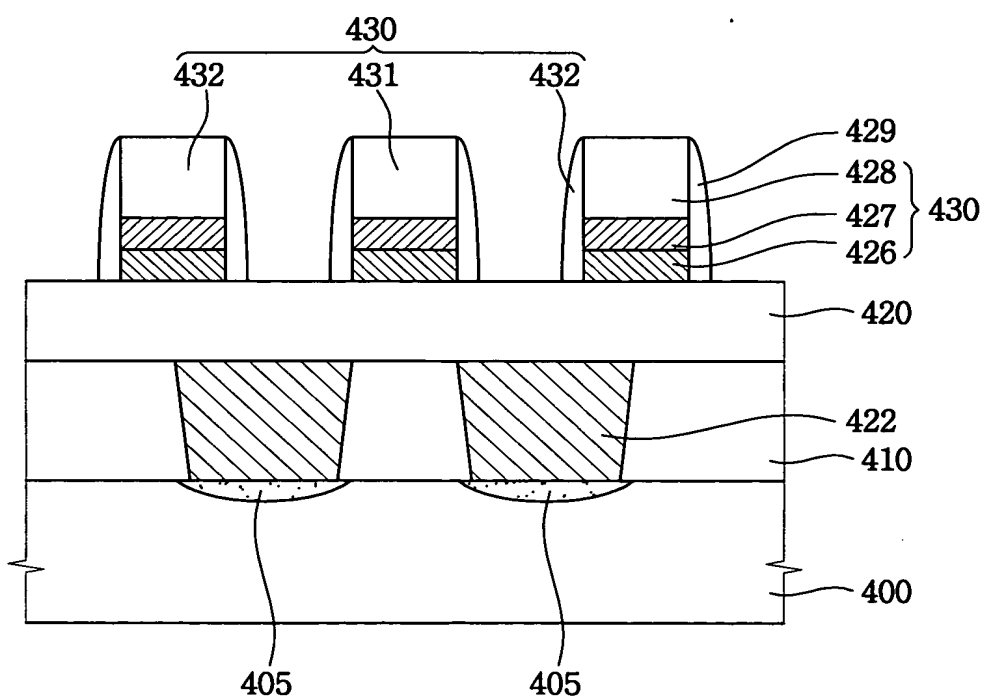




FIG. 4C

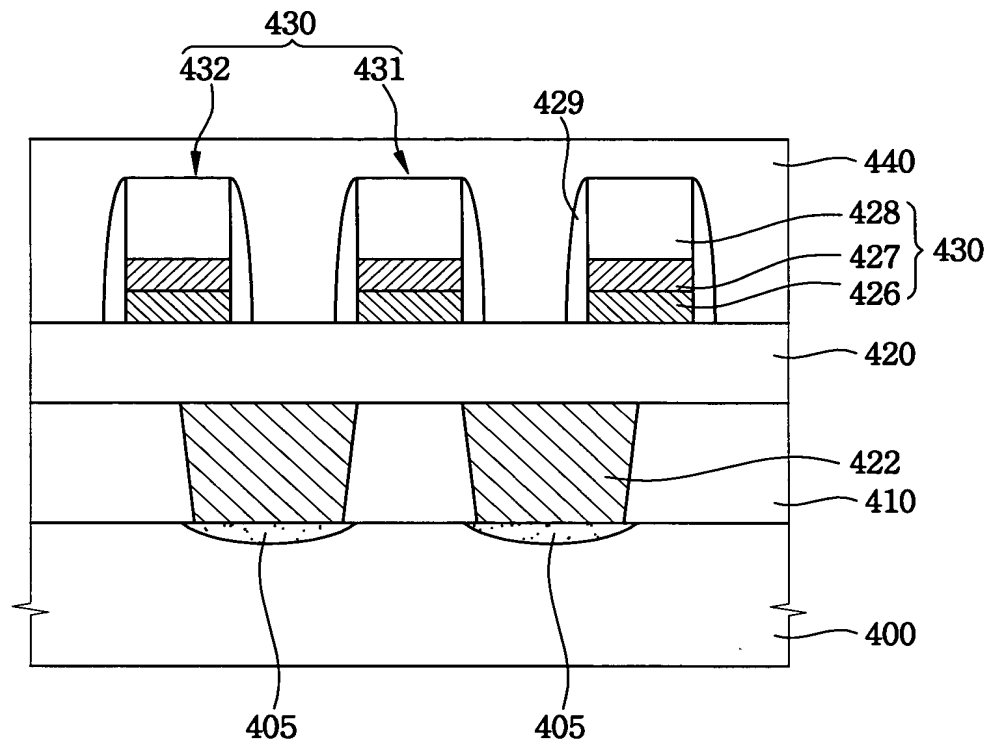


FIG. 4D

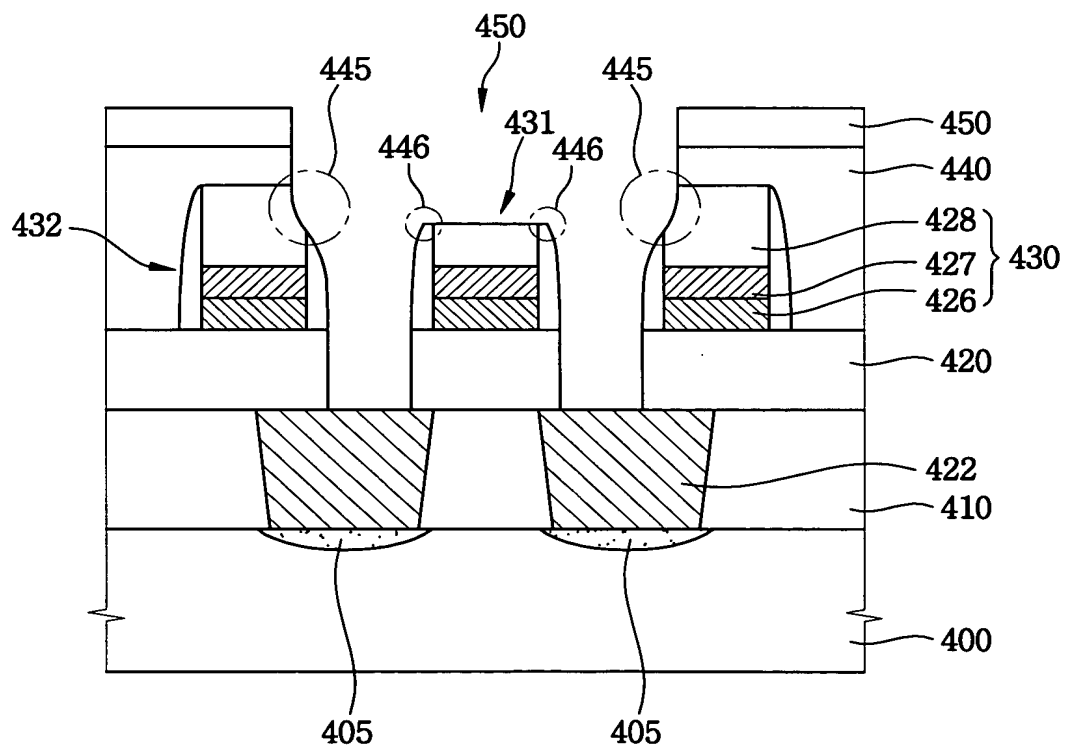


FIG. 4E

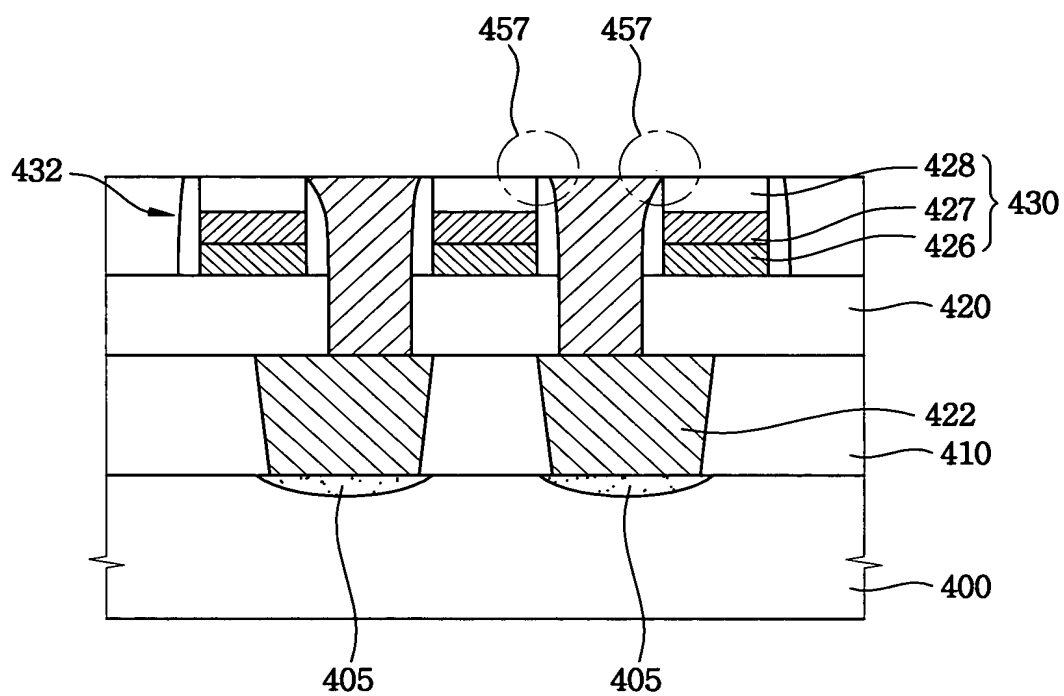


FIG. 4F

